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EXAMINER	
CLEARY, THOMAS J	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/866,005	Applicant(s) SCHMISSEUR ET AL.	
	Examiner Thomas J. Cleary	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4, 5, 9, 10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,073,253 to Nordstrom et al. ("Nordstrom") and US Patent Number 6,212,587 to Emerson et al. ("Emerson").

3. In reference to Claim 1, Nordstrom teaches a peripheral device adapted to define a plurality of device functions accessible through a data interface with a data bus (See Figure 2B Number 260); and a second processing system adapted to communicate with a second device function defined by the peripheral device through the data interface (See Figure 2A). Nordstrom does not teach a first processing system adapted to communicate with a first device function defined by the peripheral device through the data interface. Emerson teaches a first processing system that controls a selection of devices on a segment of a PCI bus (analogous to functions in a device) (See Figure 1 Number 290 and Column 4 Lines 30-44) and a second processing system that controls

a selection of devices different from those controlled by the first processing system on a segment of a PCI bus (analogous to functions in a device) (See Figure 1 Number 250 and Column 4 Lines 6-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multifunction peripheral device system of Nordstrom with the processing systems controlling different elements of Emerson, resulting in the invention of Claim 1, in order to create a device that can more easily incorporate Intelligent Input/Output technology and realize the benefits afforded by such technology (See Column 2 Lines 33-35 of Emerson).

4. In reference to Claim 4, Nordstrom and Emerson teach the limitations as applied to Claim 1 above. Nordstrom further teaches that the second processing system is coupled to the data bus through a bridge (See Figure 2B Number 210). Nordstrom does not teach that the first processing system is a peripheral device. Emerson further teaches that the first processing system is a peripheral device (See Figure 1 Number 290).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multifunction peripheral device system of Nordstrom with the processing systems controlling different elements of Emerson, resulting in the invention of Claim 4, in order to create a device that can more easily incorporate Intelligent Input/Output technology and realize the benefits afforded by such technology (See Column 2 Lines 33-35 of Emerson).

5. In reference to Claim 5, Nordstrom and Emerson teach the limitations as applied to Claim 1 above. Nordstrom does not teach that the first processing system comprises logic to cause the peripheral device to conceal one or more device functions from the second processing system while enabling the second processing system to communicate with at least one unconcealed device function defined by the peripheral device. Emerson teaches that the first processing system comprises logic to conceal one or more device functions from the second processing system (See Column 4 Lines 30-44); and that both the hidden and non-hidden elements are on the same section of bus, and thus the second processing system can communicate with the non-hidden elements while the remaining elements are hidden (See Figure 1 and Column 4 Lines 15-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multifunction peripheral device system of Nordstrom with the processing systems controlling different elements of Emerson, resulting in the invention of Claim 5, in order to create a device that can more easily incorporate Intelligent Input/Output technology and realize the benefits afforded by such technology (See Column 2 Lines 33-35 of Emerson).

6. In reference to Claim 9, Nordstrom teaches a peripheral device adapted to define a plurality of device functions coupled to a data interface of a data bus (See Figure 2B Number 260); and a second processing system (See Figure 2A). Nordstrom does not

teach initiating a first enumeration procedure at a first processing system adapted to enumerate a first device function defined by a peripheral device through the data interface; and initiating a second enumeration procedure at a second processing system adapted to enumerate a second device function of peripheral device through the data interface. Emerson teaches a first processing system that controls a selection of devices on a segment of a PCI bus (analogous to functions in a device) (See Figure 1 Number 290 and Column 4 Lines 30-44); enumerating a first device function defined by a peripheral device by a first processing system (See Column 3 Lines 13-17); and enumerating a second device function defined by a peripheral device by a second processing system (See Column 3 Lines 11-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multifunction peripheral device system of Nordstrom with the processing systems controlling different elements of Emerson, resulting in the invention of Claim 9, in order to create a device that can more easily incorporate Intelligent Input/Output technology and realize the benefits afforded by such technology (See Column 2 Lines 33-35 of Emerson).

7. In reference to Claim 10, Nordstrom and Emerson teach the limitations as applied to Claim 9 above. Nordstrom further teaches that all of the functions in the devices are I/O Device Adapters (See Figure 2B), so it is inherent that at least one of the enumerated device functions is associated with an I/O channel.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multifunction peripheral device system of Nordstrom with the processing systems controlling different elements of Emerson, resulting in the invention of Claim 10, in order to create a device that can more easily incorporate Intelligent Input/Output technology and realize the benefits afforded by such technology (See Column 2 Lines 33-35 of Emerson).

8. In reference to Claim 12, Nordstrom and Emerson teach the limitations as applied to Claim 9 above. Nordstrom further teaches that the second processing system is coupled to the data bus through a bridge (See Figure 2B Number 210). Nordstrom does not teach that the first processing system is a peripheral device. Emerson further teaches that the first processing system is a peripheral device (See Figure 1 Number 290).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multifunction peripheral device system of Nordstrom with the processing systems controlling different elements of Emerson, resulting in the invention of Claim 14, in order to create a device that can more easily incorporate Intelligent Input/Output technology and realize the benefits afforded by such technology (See Column 2 Lines 33-35 of Emerson).

9. In reference to Claim 13, Nordstrom and Emerson teach the limitations as applied to Claim 9 above. Nordstrom does not teach causing the peripheral device to

conceal one or more device functions from the second processing system while enabling the second processing system to communicate with at least one unconcealed device function defined by the peripheral device. Emerson teaches concealing one or more device functions from the second processing system (See Column 4 Lines 30-44); and that both the hidden and non-hidden elements are on the same section of bus, and thus the second processing system can communicate with the non-hidden elements while the remaining elements are hidden (See Figure 1 and Column 4 Lines 15-17).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multifunction peripheral device system of Nordstrom with the processing systems controlling different elements of Emerson, resulting in the invention of Claim 13, in order to create a device that can more easily incorporate Intelligent Input/Output technology and realize the benefits afforded by such technology (See Column 2 Lines 33-35 of Emerson).

10. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstrom and Emerson as applied to Claim 1 above, and further in view of US Patent Number 6,230,216 to Chambers et al. ("Chambers").

11. In reference to Claim 2, Nordstrom and Emerson teach the limitations as applied to Claim 1 above. Nordstrom further teaches that all of the functions in the devices are I/O Device Adapters (See Figure 2B), so it is inherent that all of the enumerated device functions are associated with an I/O channel. Nordstrom and Emerson do not teach the

first processing system comprising logic to enumerate each device function associated with an I/O channel. Chambers teaches a processor that enumerates devices on a bus based on the configuration requirements those devices have (See Column 6 Lines 24-40).

One of ordinary skill in the art at the time the invention was made would combine the device of Nordstrom and Emerson with the enumeration processor of Chambers, resulting in the invention of Claim 2, in order to be in accordance with the PCI specification (See Column 6 Lines 24-25 of Chambers).

12. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstrom, Emerson, and Chambers as applied to Claim 2 above, and further in view of US Patent Number 6,044,207 to Pecone et al. ("Pecone").

13. In reference to Claim 3, Nordstrom, Emerson, and Chambers teach the limitations as applied to Claim 2 above. Nordstrom, Emerson, and Chambers do not teach that the device function associated with the I/O channel comprises logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

One of ordinary skill in the art at the time the invention was made would combine the device of Emerson and Chambers with the peripheral RAID device of Pecone, resulting in the invention of Claim 3, in order to provide the ability to connect a high performance external storage system that allows for managing multiple independent

disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

14. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstrom and Emerson as applied to Claims 5 and 13 above, and further in view of US Patent Number 6,647,434 to Kamepalli (Kamepalli).

15. In reference to Claim 6, Nordstrom and Emerson teach the limitations as applied to Claim 5 above. Emerson further teaches logic to enumerate a first device function defined by the peripheral device (See Column 3 Lines 8-10 and 15-17). Nordstrom and Emerson do not teach logic to set information in a configuration header maintained at the peripheral device to conceal the first device function from the second processing system. Kamepalli teaches the BIOS sending a signal to a register in a peripheral device header that indicates whether the device is enabled and can communicate with the CPU or disabled and cannot communicate with the CPU (See Column 3 Lines 55-67 and Column 4 Lines 1-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nordstrom and Emerson with the device header system of Kamepalli, resulting in the invention of Claim 6, in order to allow a

hidden function to be made visible without rebooting the system (See Column 4 Lines 33-36 of Kamepalli).

16. In reference to Claim 14, Nordstrom and Emerson teach the limitations as applied to Claim 13 above. Emerson further teaches enumerating a first device function defined by the peripheral device (See Column 3 Lines 8-10 and 15-17). Nordstrom and Emerson do not teach setting information in a configuration header maintained at the peripheral device to conceal the first device function from the second processing system. Kamepalli teaches the BIOS sending a signal to a register in a peripheral device header that indicates whether the device is enabled and can communicate with the CPU or disabled and cannot communicate with the CPU (See Column 3 Lines 55-67 and Column 4 Lines 1-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nordstrom and Emerson with the device header system of Kamepalli, resulting in the invention of Claim 14, in order to allow a hidden function to be made visible without rebooting the system (See Column 4 Lines 33-36 of Kamepalli).

17. Claims 7, 8, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstrom and Emerson as applied to Claims 5 and 13 above, and further in view of US Patent Number 5,734,847 to Garbus et al. ("Garbus").

18. In reference to Claim 7, Nordstrom and Emerson teach the limitations as applied to Claim 5 above. Nordstrom further teaches a bridge coupled to the peripheral device through a secondary bus (See Figure 2B Number 210). Nordstrom does not teach that the bridge comprises logic to initiate execution of an enumeration process by the first processing system prior to completion of an enumeration process by the second processing system. Emerson further teaches a bridge coupled to the peripheral device through a secondary bus (See Figure 1 Number 210). Garbus teaches a bridge that comprises logic to initiate execution of an enumeration process by the first processing system prior to completion of an enumeration process by the second processing system (See Figure 6 Numbers 211 and 215 and Column 11 Lines 35-57).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nordstrom and Emerson with the enumeration logic and procedure of Garbus, resulting in the invention of Claim 7, in order to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus).

19. In reference to Claim 8, Nordstrom and Emerson teach the limitations as applied to Claim 5 above. Nordstrom and Emerson do not teach that the first processing system comprises logic to transmit a signal to the peripheral device to inhibit enumeration of the peripheral device by the second processing system. Garbus teaches that the first processing system transmitting a signal to the peripheral device to

inhibit enumeration of the peripheral device by the second processing system (See Figure 3b and Column 7 Lines 46-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nordstrom and Emerson with the bit masking, enumeration logic, and procedure of Garbus, resulting in the invention of Claim 8, in order allow the hidden devices to be masked from detection by the processor (See Column 7 Lines 59-61 of Garbus); and to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus).

20. In reference to Claim 15, Nordstrom and Emerson teach the limitations as applied to Claim 13 above. Nordstrom further teaches a bridge coupled to the peripheral device through a secondary bus (See Figure 2B Number 210). Nordstrom does not teach initiating execution of an enumeration process by the first processing system prior to completion of an enumeration process by the second processing system. Emerson further teaches a bridge coupled to the peripheral device through a secondary bus (See Figure 1 Number 210). Garbus teaches initiating execution of an enumeration process by the first processing system prior to completion of an enumeration process by the second processing system (See Figure 6 Numbers 211 and 215 and Column 11 Lines 35-57).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nordstrom and Emerson with the

enumeration logic and procedure of Garbus, resulting in the invention of Claim 7, in order to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus).

21. In reference to Claim 16, Nordstrom and Emerson teach the limitations as applied to Claim 13 above. Nordstrom and Emerson do not teach transmitting a signal to the peripheral device to inhibit enumeration of the peripheral device by the second processing system. Garbus teaches transmitting a signal to the peripheral device to inhibit enumeration of the peripheral device by the second processing system (See Figure 3b and Column 7 Lines 46-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nordstrom and Emerson with the bit masking, enumeration logic, and procedure of Garbus, resulting in the invention of Claim 16, in order allow the hidden devices to be masked from detection by the processor (See Column 7 Lines 59-61 of Garbus); and to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus).

22. Claims 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstrom and Emerson as applied to Claims 10 and 22 above, and further in view of Pecone.

23. In reference to Claim 11, Nordstrom and Emerson teach the limitations as applied to Claim 10 above. Nordstrom and Emerson do not teach that the device function associated with the I/O channel comprises logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

One of ordinary skill in the art at the time the invention was made would combine the device of Emerson and Chambers with the peripheral RAID device of Pecone, resulting in the invention of Claim 11, in order to provide the ability to connect a high performance external storage system that allows for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

24. In reference to Claim 23, Nordstrom and Emerson teach the limitations as applied to Claim 22 above. Nordstrom and Emerson do not teach that the device function associated with the I/O channel comprises logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

One of ordinary skill in the art at the time the invention was made would combine the device of Emerson and Chambers with the peripheral RAID device of Pecone, resulting in the invention of Claim 23, in order to provide the ability to connect a high

performance external storage system that allows for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

25. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstrom, Emerson, Garbus, and US Patent Number 5,737,344 to Belser et al. ("Belser").

26. In reference to Claim 17, Nordstrom teaches a peripheral device adapted to define a plurality of device functions coupled to a data interface of a data bus (See Figure 2B Number 260); and a second processing system (See Figure 2A). Nordstrom does not teach initiating a first enumeration procedure at a first processing system adapted to enumerate a first device function defined by a peripheral device through the data interface; initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling at last one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure; and a storage medium comprising machine-readable instructions. Emerson teaches a first processing system that controls a selection of devices on a segment of a PCI bus (analogous to functions in a device) (See Figure 1 Number 290 and Column 4 Lines 30-44); and enumerating a first device

function defined by a peripheral device by a first processing system (See Column 3 Lines 13-17). Garbus teaches initiating a bus transaction on the data bus to cause the first element to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure (See Figure 6 Numbers 211 and 215 and Column 11 Lines 35-57). Belser teaches a processor that executes machine-readable instructions stored on a direct access storage device (See Column 4 Lines 5-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multifunction peripheral device system of Nordstrom with the processing systems controlling different elements of Emerson, the enumeration procedure of Garbus, and the storage medium comprising machine-readable instructions of Belser, resulting in the invention of Claim 17, in order to create a device that can more easily incorporate Intelligent Input/Output technology and realize the benefits afforded by such technology (See Column 2 Lines 33-35 of Emerson); to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus); and in to provide an increased robustness against losing the instructions necessary to operate the device (See Column 2 Lines 43-45 of Belser).

27. In reference to Claim 18, Nordstrom, Emerson, Garbus, and Belser teach the limitations as applied to Claim 17 above. Nordstrom further teaches that all of the

functions in the devices are I/O Device Adapters (See Figure 2B), so it is inherent that the first of the enumerated device functions is enumerated as an I/O channel.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multifunction peripheral device system of Nordstrom with the processing systems controlling different elements of Emerson, the enumeration procedure of Garbus, and the storage medium comprising machine-readable instructions of Belser, resulting in the invention of Claim 18, in order to create a device that can more easily incorporate Intelligent Input/Output technology and realize the benefits afforded by such technology (See Column 2 Lines 33-35 of Emerson); to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus); and in to provide an increased robustness against losing the instructions necessary to operate the device (See Column 2 Lines 43-45 of Belser).

28. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstrom, Emerson, Garbus, and Belser as applied to Claim 18 above, and further in view of Pecone.

29. In reference to Claim 19, Nordstrom, Emerson, Garbus, and Belser teach the limitations as applied to Claim 18 above. Nordstrom, Emerson, Garbus, and Belser do not teach the device function associated with the I/O channel comprising logic to

communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

One of ordinary skill in the art at the time the invention was made would combine the device of Nordstrom, Emerson, Garbus, and Belser with the peripheral RAID device of Pecone, resulting in the invention of Claim 19, in order to provide the ability to connect a high performance external storage system that allows for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

30. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstrom, Emerson, Garbus, and Belser as applied to Claim 17 above, and further in view of Kamepalli.

31. In reference to Claim 20, Nordstrom, Emerson, Garbus, and Belser teach the limitations as applied to Claim 17 above. Nordstrom, Emerson, Garbus, and Belser do not teach initiating a bus transaction to set information in a configuration header maintained at the peripheral device to conceal the first device function from subsequent enumeration procedures. Kamepalli teaches the BIOS sending a signal to a register in a peripheral device header that indicates whether the device is enabled and can

communicate with the CPU or disabled and cannot communicate with or be enumerated by the CPU (See Column 3 Lines 55-67 and Column 4 Lines 1-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nordstrom, Emerson, Garbus, and Belser with the device header system of Kamepalli, resulting in the invention of Claim 14, in order to allow a hidden function to be made visible without rebooting the system (See Column 4 Lines 33-36 of Kamepalli).

32. Claims 21, 22, 26, and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstrom, Emerson, and Garbus.

33. In reference to Claim 21, Nordstrom teaches a peripheral device adapted to define a plurality of device functions coupled to a data interface of a data bus (See Figure 2B Number 260); and a second processing system (See Figure 2A). Nordstrom does not teach logic to initiate a first enumeration procedure to enumerate a first device function defined by a peripheral device; initiating a second enumeration procedure at a second processing system adapted to enumerate a second device function of peripheral device through the data interface; and logic to initiate a bus transaction on the data bus causing the first device function to be concealed from subsequent enumeration procedures while enabling the subsequent enumeration procedures to access at least one other device function defined by the peripheral device. Emerson teaches a first processing system that controls a selection of devices on a segment of a PCI bus

(analogous to functions in a device) (See Figure 1 Number 290 and Column 4 Lines 30-44); and enumerating a first device function defined by a peripheral device by a first processing system (See Column 3 Lines 13-17). Garbus teaches initiating a bus transaction on the data bus to cause the first element to be concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure (See Figure 6 Numbers 211 and 215 and Column 11 Lines 35-57).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multifunction peripheral device system of Nordstrom with the processing systems controlling different elements of Emerson and the enumeration procedure of Garbus, resulting in the invention of Claim 21, in order to create a device that can more easily incorporate Intelligent Input/Output technology and realize the benefits afforded by such technology (See Column 2 Lines 33-35 of Emerson); and to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus).

34. In reference to Claim 22, Nordstrom, Emerson, and Garbus teach the limitations as applied to Claim 21 above. Nordstrom further teaches that all of the functions in the devices are I/O Device Adapters (See Figure 2B), so it is inherent that the first of the enumerated device functions is enumerated as an I/O channel.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multifunction peripheral device system of Nordstrom

with the processing systems controlling different elements of Emerson, resulting in the invention of Claim 21, in order to create a device that can more easily incorporate Intelligent Input/Output technology and realize the benefits afforded by such technology (See Column 2 Lines 33-35 of Emerson); and to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus).

35. In reference to Claim 26, Nordstrom teaches a peripheral device adapted to define a plurality of device functions coupled to a data interface of a data bus (See Figure 2B Number 260); and a second processing system (See Figure 2A). Nordstrom does not teach initiating a first enumeration procedure at a first processing system adapted to enumerate a first device function defined by a peripheral device through the data interface; and initiating a bus transaction on the data bus to cause the first device function to be concealed from subsequent enumeration procedures while enabling at last one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure. Emerson teaches a first processing system that controls a selection of devices on a segment of a PCI bus (analogous to functions in a device) (See Figure 1 Number 290 and Column 4 Lines 30-44); enumerating a first device function defined by a peripheral device by a first processing system (See Column 3 Lines 13-17); and enumerating a second device function defined by a peripheral device by a second processing system (See Column 3 Lines 11-13). Garbus teaches initiating a bus transaction on the data bus to cause the first element to be

concealed from subsequent enumeration procedures while enabling at least one other device function defined by the peripheral device to be enumerated by a subsequent enumeration procedure (See Figure 6 Numbers 211 and 215 and Column 11 Lines 35-57).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multifunction peripheral device system of Nordstrom with the processing systems controlling different elements of Emerson and the enumeration procedure of Garbus, resulting in the invention of Claim 21, in order to create a device that can more easily incorporate Intelligent Input/Output technology and realize the benefits afforded by such technology (See Column 2 Lines 33-35 of Emerson); and to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus).

36. In reference to Claim 27, Nordstrom, Emerson, and Garbus teach the limitations as applied to Claim 26 above. Nordstrom further teaches that all of the functions in the devices are I/O Device Adapters (See Figure 2B), so it is inherent that the first of the enumerated device functions is enumerated as an I/O channel.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the multifunction peripheral device system of Nordstrom with the processing systems controlling different elements of Emerson and the enumeration procedure of Garbus, resulting in the invention of Claim 21, in order to create a device that can more easily incorporate Intelligent Input/Output technology and

realize the benefits afforded by such technology (See Column 2 Lines 33-35 of Emerson); and to prevent the host processor from loading drivers or allocating address space to elements that are to be hidden (See Column 2 Lines 18-21 of Garbus).

37. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstrom, Emerson, and Garbus as applied to Claim 21 above, and further in view of Kamepalli.

38. In reference to Claim 24, Nordstrom, Emerson, and Garbus teach the limitations as applied to Claim 21 above. Nordstrom, Emerson, and Garbus do not teach that the processing system further comprises logic to initiate a bus transaction to set information in a configuration header maintained at the peripheral device to conceal the first device function from subsequent enumeration procedures. Kamepalli teaches the BIOS sending a signal to a register in a peripheral device header that indicates whether the device is enabled and can communicate with the CPU or disabled and cannot communicate with or be enumerated by the CPU (See Column 3 Lines 55-67 and Column 4 Lines 1-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nordstrom, Emerson, and Garbus with the device header system of Kamepalli, resulting in the invention of Claim 24, in order to allow a hidden function to be made visible without rebooting the system (See Column 4 Lines 33-36 of Kamepalli).

39. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstrom, Emerson, Garbus, and Kamepalli as applied to Claim 24 above, and further in view of US Patent Number 5,960,213 to Wilson ("Wilson").

40. In reference to Claim 25, Nordstrom, Emerson, Garbus, and Kamepalli teach the limitations as applied to Claim 24 above. Nordstrom further teaches that the data bus is a PCI bus (See Figure 2B Number 230). Nordstrom, Emerson, Garbus, and Kamepalli do not teach that the processing system further comprising logic to initiate a bus transaction to modify data in a Header Type register of the configuration header. Wilson teaches a unit that sends signals to set a bit in the Header Type register of the devices connected to it (See Column 6 Lines 21-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nordstrom, Emerson, Garbus, and Kamepalli with the device to set the Header Type of Wilson, resulting in the invention of Claim 25, in order to allow the host system to view the secondary PCI devices as a single multifunction device (See Column 6 Lines 7-10 of Wilson).

41. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstrom, Emerson, and Garbus as applied to Claim 27 above, and further in view of Pecone.

42. In reference to Claim 28, Nordstrom, Emerson, and Garbus teach the limitations as applied to Claim 27 above. Nordstrom, Emerson, and Garbus do not teach the device function associated with the I/O channel comprising logic to communicate with a RAID channel. Pecone teaches that one of the devices that can be connected to a PCI bus is a RAID device (See Column 4 Lines 7-16).

One of ordinary skill in the art at the time the invention was made would combine the device of Nordstrom, Emerson, and Garbus with the peripheral RAID device of Pecone, resulting in the invention of Claim 28, in order to provide the ability to connect a high performance external storage system that allows for managing multiple independent disks in a manner that achieves a desired level of availability, efficiency, capacity, performance, and economic cost of storing large quantities of readily available data in the data storage system (See Column 4 Lines 16-24) and because RAID systems are commonly used to provide system backups.

43. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nordstrom, Emerson, and Garbus as applied to Claim 26 above, and further in view of Kamepalli.

44. In reference to Claim 29, Nordstrom, Emerson, and Garbus teach the limitations as applied to Claim 26 above. Nordstrom, Emerson, and Garbus do not teach initiating a bus transaction to set information in a configuration header maintained at the peripheral device to conceal the first device function from subsequent enumeration

procedures. Kamepalli teaches the BIOS sending a signal to a register in a peripheral device header that indicates whether the device is enabled and can communicate with the CPU or disabled and cannot communicate with or be enumerated by the CPU (See Column 3 Lines 55-67 and Column 4 Lines 1-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Nordstrom, Emerson, and Garbus with the device header system of Kamepalli, resulting in the invention of Claim 29, in order to allow a hidden function to be made visible without rebooting the system (See Column 4 Lines 33-36 of Kamepalli).

Response to Arguments

45. Applicant's arguments with respect to Claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (7-4:30), Alt. Fridays (7-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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tjc

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